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the program is, in effect, activated by
reading the xe2x80x9cexchange-
addressxe2x80x9d into memory
during initialization, i.e., when the xe2
x80x9cexchange-addressxe2x80x9d
is read by the I2C controller into the
EEPROM where it is stored as part of
the calibration data. The I2C controller
is then used to read the stored xe2x8
0x9cexchange-addressxe2x80x9d and
the calibration data is read from the
EEPROM. The I2C controller then uses
the calibration data to identify which
of several SRAM cells contain a
configuration bit. The reading of the
calibration data is performed

simultaneously with the reading of the exchange-address because the same address line is used for both operations, and the SRAM is accessed in a byte-wide fashion. Thus, no such problem would result if the I2C controller only reads the exchange-address and uses the calibration data to determine which bit locations should be programmed, since no other addresses could be read. However, because the same address is used for the calibration data operation, it would be possible for a glitch to accidentally initialize the chip in an undesirable state, and the calibration data would not necessarily store an accurate indication of the desired state. The prior art method of reading

calibration data also limits the flexibility of the EEPROM by requiring that it be accessed in a byte-wide fashion. Thus, although only a small number of bit locations, on the order of one byte, are read by the calibration code in order to determine the actual storage configuration, the fact that the reading is done in a byte-wide fashion requires that each byte be read in order to determine the correct state of a bit location, thereby increasing the time required to perform a calibration. The synchronization of the reading of the calibration data and the calibration locations of interest is particularly difficult in circuits where the calibration data is

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